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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,187	10/20/2003	N. Johan Knall	MA-002-1-I-a	2700

7590 11/16/2005

MATRIX SEMICONDUCTOR
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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/689,187	KNALL ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/16/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,396 to Zhang (hereafter Zhang '396) in view of U.S. Patent No. 6,111,302 to Zhang et al. (hereafter Zhang '302).

Zhang '396 discloses a three dimensional multi-level memory array (figure 1) disposed above a substrate (10), the array comprising: a first plurality of spaced apart rail stacks (bottom electrode 503 + TiW barrier layer disposed thereon, or alternately, layers 503 and 502cb in figures 10a,b) disposed at a first height in a first direction above the substrate (see figure 6A and figure 1); a second plurality of rail stacks (top electrode 501+ TiW barrier layer disposed

thereon, or alternately, layers 501 and 502ca in figures 10a,b) disposed above the first height and in a second direction different from the first direction (figures 1 and 6A) and a plurality of memory cells (formed from 501, 502, and 503 at the relative intersections of 501 and 503), each memory cell comprising an antifuse (502; see column 7, lines 10-18; also see column 6, lines 18-35, noting that thin layers of intrinsic amorphous silicon act as an antifuse), wherein the antifuses are disposed at the intersections of the rail stacks (see figure 6A).

Zhang '396 fails to specify that silicon nitride could be used as the metal-to-metal antifuse material.

Zhang '302 teaches that silicon nitride is an appropriate material for use as a metal-to-metal antifuse, and that it may be used interchangeably with other known antifuse materials, such as amorphous silicon (see column 3, lines 39-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the amorphous silicon antifuse layer of Zhang '396, such that it is silicon nitride, as suggested by Zhang '302. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use silicon nitride for the metal-to-metal antifuse, because Zhang '302 shows that both silicon nitride and amorphous silicon are considered art recognized equivalents that may be used interchangeably (Zhang '302 – column 3, lines 39-56), and that both materials provide the advantages of eliminating switch-off phenomena and improving the on and off-state properties of the antifuse (see Zhang '302, column 2, lines 14-33). A person skilled in the art would further appreciate that since both Zhang '302 and Zhang '396 are directed toward metal-to-metal antifuses using generally similar materials with similar programming voltages (Zhang '302, column 6, lines 40-45; Zhang '396, column 8, lines 60-67),

it would be reasonable and apparent to apply any of the specific antifuse materials in Zhang '302 to the structure of Zhang '396.

4. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,835,396 to Zhang in view of U.S. Patent No. 4,881,114 to Mohsen et al.

Regarding claim 1, Zhang discloses a three dimensional multi-level memory array (figure 1) disposed above a substrate (10), the array comprising: a first plurality of spaced-apart rail stacks (see figure 10a, formed from layers 503 and 502cb) disposed at a first height in a first direction above the substrate (see figures 1 and 10a; column 10, lines 7-12, noting that layers 503 and 502cb are patterned together in a rail shape); a second plurality of spaced apart rail stacks (formed from layers 502ca and 501); a plurality of memory cells (formed from 501,502ca,502cc,502cb and 503 at the intersection of the first and second rails; also see figures 1, 7, and 12), each memory cell comprising an antifuse (502ca), wherein the antifuses are disposed at the intersections of the first and second rail stacks (antifuses are disposed on the bottom of and across the entire extent of the second rail stack, and thus, are present at the intersection of the two rail stacks – see figure 10A).

Zhang fails to disclose that the antifuse is formed of silicon nitride.

Mohsen discloses a memory cell having a silicon nitride antifuse (14; see column 4, lines 22-25) disposed between layers comprising either metal or semiconductor materials (column 4, lines 4-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the antifuse of Zhang, such that it is formed of silicon nitride, as taught by Mohsen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use silicon nitride as the antifuse, because Mohsen shows that silicon nitride is an appropriate antifuse for use between metal electrodes or metal and semiconductor electrodes (Mohsen, column 4, lines 4-10), and that silicon nitride used as an antifuse has the advantageous properties of high reliability in the programmed and unprogrammed state, controllable antifuse rupturing properties, and high conductivity after programming (see Mohsen, column 2, lines 29-40).

Regarding claim 2, Zhang discloses that the array comprises polysilicon pn diodes (column 6, lines 50-55), and that it is desirable for the quasi-conduction layer (which is formed by the polysilicon pn diodes) to have the characteristic of having a low resistance current path when subjected to a sufficiently high forward bias, a high resistance path when subjected to a low forward bias or a reverse bias (column 6, lines 8-17; also see figure 8), and as large as possible of a nonlinear IV response in order to improve storage capacity (see column 6, lines 50-62 and column 8, line 55- column 9, line 7).

Zhang is silent as to the doping levels in the pn junction diode.

Mohsen suggests that the diode is formed from a heavily doped layer adjoining a moderately doped opposite conductivity layer (column 3, lines 45-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the doping levels of the pn junction diode of Zhang are consistent with a p+n or p-n+ device, as suggested by Mohsen. The rationale is as follows: A person having

ordinary skill in the art would have been motivated to use a pn diode with one highly doped side (i.e. p+n) because it is well established in the semiconductor device arts that such a device will have increased current flow for each bias level, which appropriately corresponds to the conditions disclosed by Zhang as most desirable, and would result in a lower resistance current path for forward bias, generally insignificant changes to the reverse bias characteristic, and greater nonlinearity of the IV response, as is appreciated by a person having skill in the art. It is expected that even lacking knowledge of the properties of p+n diodes, Zhang would arrive at a p+n structure through routine optimization of the doping levels for the diode to achieve the properties listed supra. Since Mohsen further indicates that a p+n diode portion is compatible with anti-fuse type memory cells and can function to drive and direct the current through the antifuse memory cell, a person skilled in the art would further conclude that it would be reasonable to select a p+n diode for a memory cell diode structure. Although Zhang is silent as to the specific doping levels, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Response to Arguments

5. Applicant's arguments with respect to claims 1 and 2 have been considered but are moot in view of the new grounds of rejection.

The Examiner notes in the 8/16/05 Remarks section, the Applicants appear to argue that the references applied in the previous office action (Mohsen and Zhang) do not disclose the rail stacks as claimed. The Examiner points out that since the specification does not provide a specific definition of rail stacks, but rather just examples and embodiments using rail stacks, the claim term is interpreted by its common and ordinary meaning: a stack of at least two materials or material layers formed in a rail shape. Since Zhang indicates that the rails comprise a refractory metal layer coated with a barrier layer, such a structure is considered to read on a "rail stack." Similarly, the structures in figures 10a and 10b of Zhang, having multiple layers in a rail-shaped stack (i.e. 501 and 502ca form a rail; likewise, 503 and 502cb form a rail), are considered to read on the claimed "rail stacks."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800